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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,876	02/20/2002	David J. Hathaway	FIS920010383US1	6308

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INTERNATIONAL BUSINESS MACHINES CORPORATION  
DEPT. 18G  
BLDG. 300-482  
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EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/078,876

Applicant(s)

HATHAWAY ET AL.

Examiner

Joseph D. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 November 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-12, 14-17 and 19-23 is/are rejected.  
7) ☒ Claim(s) 13 and 18 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 20 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Objections***

1. In view of the Amendment filed 11/19/2004, the Examiner withdraws all previous objections to claims 1-23.

### ***Claim Rejections - 35 USC § 112***

2. In view of the Amendment filed 11/19/2004, the Examiner withdraws all previous rejections to claims 1-23.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-12, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patra; Priyadarsan et al. (US 6529861 B1) in view of Chakradhar et al. (S. T. Chakradhar, A. Balakrishnan, and V. D. Agrawal, "An exact algorithm for selecting partial scan flip-flops", Design Automation Conference, pages 81-86, 1994, hereafter referred to as Chakradhar).

35 U.S.C. 103(a) rejection of claims 1 and 23.

Patra teaches a method for reducing switching activity during a test scan operation of at least one scan chain in an integrated circuit (the Abstract in Patra teaches a method for reducing switching activity in domino circuits; col. 7, lines 1-48 in Patra teaches an exemplary embodiment whereby the domino circuit is a scan chain made up of partial scan scan flip flops and the sequential domino logic blocks of the domino circuit are the partial scan flip-flops, i.e., memory elements, used for testing an IC chip) comprising the steps of: a. determining stimulus and result value probabilities for a plurality of memory elements in said IC (col. 3, lines 58-62, Patra teach that signal probability is the probability that the logical output is high in response to a stimulus at the input, hence signal probabilities are stimulus and result value probabilities and Step 802 in Figure 8 of Patra is a means for determining stimulus and result value probabilities for sequential domino logic blocks, i.e., partial scan flip-flops or memory elements); and b. connecting

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said memory elements to form at least one scan chain based on said probabilities, thereby reducing the switching activity as determined by the probabilities and by the ordering of said memory elements within said at least one scan chain (Figures 9a-9C & 10A-10C of Patra teach connecting said memory elements to form at least one scan chain based on said probabilities; Step 704 in Figure 7 teach power is reduced).

However Patra does not explicitly teach the specific use of a scan chain for use in testing combinational logic in an IC.

Chakradhar, in an analogous art, teaches use of a scan chain for use in testing combinational logic in an IC (see col. 1 on page 81 of Chakradhar). Note: col. 7, lines 19-48 of Patra teaches that Figures 10A-10C are an exemplary embodiment of domino circuitry whereby the Domino circuitry is Scan Circuitry modeled by an S-graph using vertices to represent flip-flops and edges to represent the connections. Col. 7, lines 19-48 of Patra clearly suggests not only the feasibility, but the desirability for the combination of Chakradhar with Patra.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patra with the teachings of Chakradhar by including use of a scan chain for use in testing combinational logic in an IC. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a scan chain for use in testing combinational logic in an IC would have provided the opportunity to reduce power consumption in scan test circuitry (see Abstract, Patra).

35 U.S.C. 103(a) rejection of claim 2.

Col. 1 on page 81 of Chakradhar teaches test generation.

35 U.S.C. 103(a) rejection of claim 3.

Col. 3, lines 55-67 in Patra teach that the signal probability  $p_g$  is the probability of a transition, therefore  $1 - p_g$  is the probability that there is no transition, hence calculating  $p_g$  is substantially the same as calculating the probability of coincidence  $1 - p_g$ .

35 U.S.C. 103(a) rejection of claim 4.

Col. 3, lines 55-67 in Patra teach that the signal probability  $p_g$  is the probability of a transition.

35 U.S.C. 103(a) rejection of claims 5, 6, 8 and 10.

If  $s_1$  denotes 103,  $s_2$  denotes 101,  $r_1$  denotes 101 and  $r_2$  denotes 102 then  $1 - p_{g1}$  denotes the probability that  $s_1 = r_1$  and  $1 - p_{g2}$  denotes the probability that  $s_2 = r_2$ , hence  $1 - p_{g1}$  is the probability that  $s_1 = s_2$  and  $1 - p_{g2}$  is the probability that  $r_1 = r_2$  since  $s_2 = r_1$ .

35 U.S.C. 103(a) rejection of claim 7, 9 and 11.

Note: if  $1 - p_{g1}$  denotes the probability that  $s_1 = r_1$  and  $1 - p_{g2}$  denotes the probability that  $s_2 = r_2$ , then  $p_{g1}$  is the probability of a transition between  $s_1$  and  $s_2$ ; and  $p_{g2}$  is the probability of a transition between  $r_1$  and  $r_2$ .

35 U.S.C. 103(a) rejection of claim 12.

One of the gates of circuit element 106 in Figure 1 of Patra teaches an inversion element between memory elements.

35 U.S.C. 103(a) rejection of claim 22.

Patra teaches a method for reducing switching activity during a test scan operation of at least one scan chain in an integrated circuit (the Abstract in Patra teaches a method for reducing switching activity in domino circuits; col. 7, lines 1-48 in Patra teaches an exemplary embodiment whereby the domino circuit is a scan chain made up of partial scan scan flip flops and the sequential domino logic blocks of the domino circuit are the partial scan flip-flops, i.e., memory elements, used for testing an IC chip) comprising the steps of: a. determining stimulus and result value probabilities for a plurality of memory elements in said IC (col. 3, lines 58-62, Patra teach that signal probability is the probability that the logical output is high in response to a stimulus at the input, hence signal probabilities are stimulus and result value probabilities and Step 802 in Figure 8 of Patra is a means for determining stimulus and result value probabilities for sequential domino logic blocks, i.e., partial scan flip-flops or memory elements); and b. connecting said memory elements to form at least one scan chain based on said probabilities, thereby reducing the switching activity as determined by the probabilities and by the ordering of said memory elements within said at least one scan chain (Figures 9a-9C &

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10A-10C of Patra teach connecting said memory elements to form at least one scan chain based on said probabilities; Step 704 in Figure 7 teach power is reduced).

However Patra does not explicitly teach the specific use of a scan chain for use in testing combinational logic in an IC.

Chakradhar, in an analogous art, teaches use of a scan chain for use in testing combinational logic in an IC (see col. 1 on page 81 of Chakradhar). Note: col. 7, lines 19-48 of Patra teaches that Figures 10A-10C are an exemplary embodiment of domino circuitry whereby the Domino circuitry is Scan Circuitry modeled by an S-graph using vertices to represent flip-flops and edges to represent the connections. Col. 7, lines 19-48 of Patra clearly suggests not only the feasibility, but the desirability for the combination of Chakradhar with Patra. Note also: Col. 1 on page 81 of Chakradhar teaches test generation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patra with the teachings of Chakradhar by including use of a scan chain for use in testing combinational logic in an IC. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a scan chain for use in testing combinational logic in an IC would have provided the opportunity to reduce power consumption in scan test circuitry (see Abstract, Patra).

5. Claims 14-17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patra; Priyadarsan et al. (US 6529861 B1) in view of Kajihara et al.



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(Seiji Kajihara, Kohei Miyase: On Identifying Don't Care Inputs of Test Patterns for Combinational Circuits. ICCAD 2001: 364-369; hereafter referred to as Kajihara).

35 U.S.C. 103(a) rejection of claims 14-17 and 19-21.

Patra substantially teaches the claimed invention described in claims 1, 3-12 (as rejected above).

However Patra does not explicitly teach the specific use of setting undetermined or don't care values to a specific value for the purposes of reducing switching activity.

Kajihara, in an analogous art, teaches use of setting undetermined or don't care values to a specific value for the purposes of reducing switching activity and compacting the test pattern set (Sections 5.1 and 5.2 in Kajihara teach setting undetermined or don't care values to a specific value for the purposes of reducing switching activity).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patra with the teachings of Kajihara by including use of setting undetermined or don't care values to a specific value for the purposes of reducing switching activity. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of setting undetermined or don't care values to a specific value for the purposes of reducing switching activity would have provided the opportunity to reduce switching activity (Section 5.2 in Kajihara).

***Allowable Subject Matter***

6. Claims 13 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD  
Primary Examiner  
Art Unit 2133

